Response to Amendment

Applicants' amendment filed on 12/23/2009 has been entered and forwarded to the

Examiner on 01/10/2010.

Therefore claims 1-5 and 18 as amended by the amendment and claims 6-17 as

previously recited are currently pending in the Application.

Allowable Subject Matter

1. Claims 1 to 10 are allowed.

2. The following is an examiner's statement of reasons for allowance:

The applied prior art of record does not disclose the presently newly added limitations of independent claims 1 to 4 , a LCD device including the a gate electrode comprising a chained metal body of nanoparticles over the one of the pair of substrates

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11 to 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yudasaka et al. (U.S. Patent Publication No. 2002/0179906, herein after Yudasaka, also cited by Applicants' in their IDS) in view of Bojkov et al. (U.S. Patent No. 5,947,783 herein after Bojkov)

With respect to claim 11, Yudasaka describes a liquid crystal display device comprising

the steps of :

(a) forming a gate electrode over a substrate having an insulating surface with a droplet

discharge method. (fig.3 # 18).

Yudasaka mentions a gate electrode but does not specifically mention it (gate) of nanoparticles.

However Bojkov a patent from the same filed of endeavor, describes in its abstract (col .5 lines 30-35) a gate electrode formed over one of the pair of substrates by fusing conductive nanoparticles to provide films that have desired pixel structures, that can be used in display structures.

Therefore it would have been obvious to one of ordinary skill in the at the time of the invention to include Bojkov's a gate electrode formed over the substrate by fusing conductive nanoparticles in Yudasak's device. The motivation for the above inclusion is to provide films that have desired pixel structures, that can be used in display structures. (Bojkov col .1 lines 43-47).

The remaining limitations of claim 11 are:

; laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode; (rejected for reasons under claims 1 to 4 above) forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching the insulating layer by using the first mask; (Yudasaka para 0183) forming a semiconductor layer containing one conductivity type impurity;(Yudasaka figs.) forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer by using the second mask (Yudasaka para 00186) forming source and drain wirings with a droplet discharge method;(Yudasaka fig.11 33s and 33d, paras 205-210) and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. (Yudasaka para 0187).

With respect to claim 12 Yudasaka describes a method for manufacturing a liquid crystal display device comprising the steps of: forming a gate electrode and a connection wiring over a substrate having an insulating surface with a droplet discharge method using a composition containing conductive nano particles ;laminating a gate insulating layer, a semiconductor layer, and an insulating
layer over the gate electrode; forming a first mask in a position overlapping with the gate electrode with a droplet discharge method; forming a channel protective layer by etching

the insulating layer by using the first mask; forming a semiconductor layer containing one conductivity type impurity; forming a second mask in a region including the gate electrode with a droplet discharge method; etching the semiconductor layer containing one conductivity type impurity and the semiconductor layer by using the second mask ; partially exposing the connection wiring by selectively etching the gate insulating layer; forming a source wiring and a drain wiring and connecting at least one of the source wiring and the drain wiring to the connection wiring at the same time; and etching the semiconductor layer containing one conductivity type impurity over the channel protective layer by using the source and drain wirings as masks. (rejected for reasons under claims 1-4 and 11).

With respect to claim 13 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the step of laminating a gate insulating layer, a semiconductor layer, and an insulating layer over the gate electrode is carried out without exposing to the atmosphere. (para 0039 e.g. CVD carried out in enclosed chamber).

With respect to claim 14 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the gate insulating film is formed by sequentially laminating by a first silicon nitride film, a silicon oxide film, and a second silicon nitride film. (Bojkov col. 13 lines 14--15).

With respect to 15 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein average particle size of the conductive nanoparticles is from 5 nm to 10 nm. (inherent nano particles by definition are in the overlapping range 1-100 nms).

With respect to 16 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the first mask is formed using a composition containing conductive nanoparticles. (Yudasaka para 0183 and figures, also disclosed in Bojkov)

With respect to claim 17 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11 or 12, wherein the second mask is formed using a composition containing conductive nanoparticles. (Yudasaka para 0183 and figures, also disclosed in Bojkov)

With respect to claim 18 Yudasaka describes the method for manufacturing a liquid crystal display device according to claim 11, wherein the source and drain wirings are formed using a composition containing conductive nanoparticles. (well known in the art, also rejected for reasons under claims12 and 16-17,see also Bojkov).

Response to Arguments

3. Applicant's arguments filed 12/23/2009 with respect to claims 11-18 have been fully considered but they are not persuasive. :

4. Applicants' contention that Yudasaka in "paragraph 183 etc." e.g. figure3 and further description in para 0133/0134 (i.e. etc. in above quotation) describes gates and for e.g. Yudasaka figs. 16 and paras 208/209 and as also stated under previous rejections of claims 1-4 etc. and incorporated by reference in to rejections of claims 11 and 12 etc. describes forming gate electrode over substrate having an insulating surface droplet discharge method using a composition containing conductive nanoparticles (Bojkov- abstract, col. 5 lines 30-35, etc.) such that one of ordinary skill in the art would understand all the presently recited limitations of claim 11 as disclosed as stated in the rejections by Yudasaka, etc.

Thus Applicants' arguments wrt claims 11-18 are not persuasive and finally rejected.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVEN H. RAO whose telephone number is (571)272-1718. The examiner can normally be reached on 8.30-5.30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Steven H Rao/
Examiner, Art Unit 2814

/Howard Weiss/
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